Synthesizer Output (635-4930-001)

Rockwell International

instructions

Collins Telecommunications Products Division

Printed in USA

523-0767971-201211
1 June 1977
2nd Revision, 1 January 1979

1. DESCRIPTION

Synthesizer Output 635-4930-001, shown in figure 1, is a module that contains a base 2-layer planar card, four rf secure compartments (metal box construction), and five printed wiring boards. The base 2-layer planar card contains a 20-pin edge-on connector (2 layers, 10 pins each).

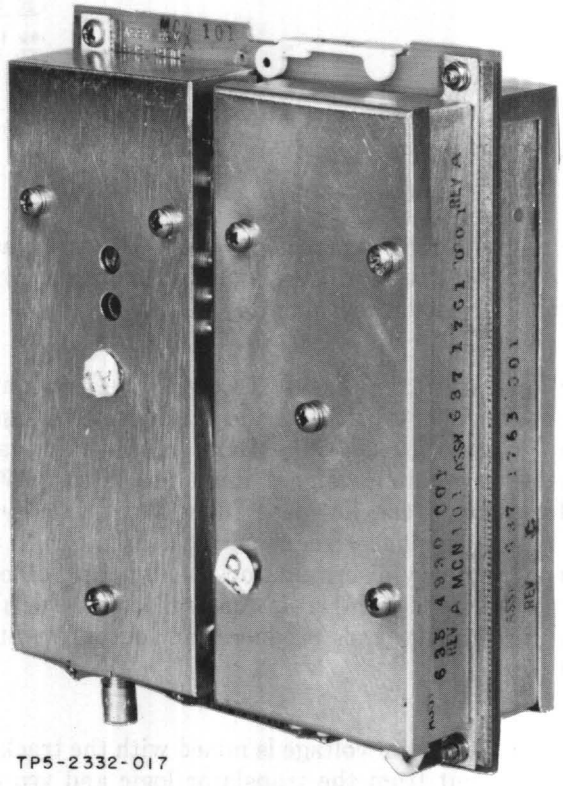
The synthesizer output module consists of translator logic, translator vco, output mixer, output logic, output vco, low-pass filter circuits, and a loss-of-lock (lol) monitor circuit.

2. PRINCIPLES OF OPERATION

2.1 General (Refer to figure 2.)

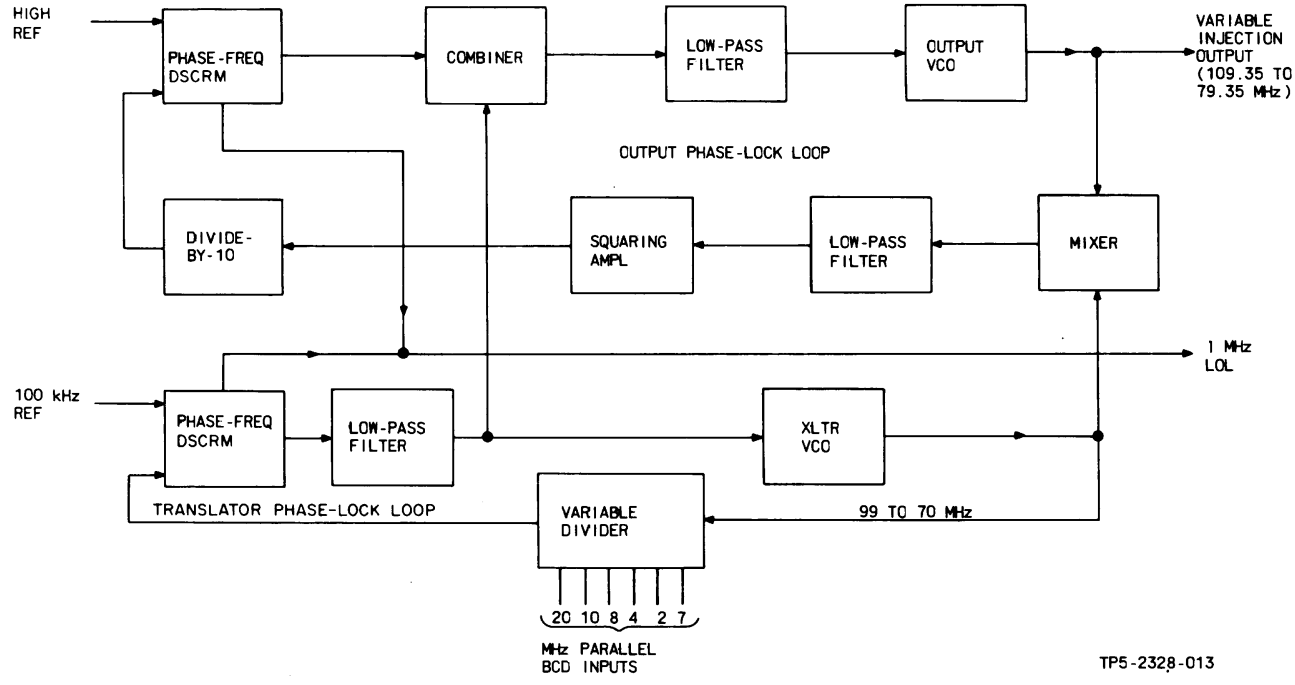
The synthesizer output module receives MHz bcd frequency control signals, a 100-kHz reference signal and a high-reference signal (1.035 to 0.935001 MHz), and generates a 109.35- to 79.35001-MHz variable injection signal output and a 1-MHz lock signal output (logic 1 for lock).

The translator logic circuits receive a 100-kHz reference input, a translator vco signal, and a bcd frequency input. The bcd frequency input is used to program a variable frequency divider (divide-by-99 to 70). The programmed variable frequency divider output (100 kHz) and the 100-kHz reference input are supplied to a phase/frequency discriminator that, with a low-pass filter, provides a control voltage proportional to the phase/frequency difference between its inputs. This control voltage is also supplied as a tracking voltage to the output phase-lock loop.



Synthesizer Output
Figure 1

The translator vco circuit receives the control voltage signal from translator logic circuits and is driven to and phase-locked at the variable frequency as programmed by variable divider bcd inputs to translator logic circuits. The translator vco output (99 to 70 MHz) is supplied to translator logic circuits for



Synthesizer Output, Block Diagram
Figure 2

clocking and lock signal generation. The translator vco output (99 to 70 MHz) is supplied to output mixer circuits for frequency mixing.

The output mixer circuit receives the translator signal input (99 to 70 MHz) and the output vco signal input (109.35 to 79.3501 MHz), mixes them and supplies a reference signal input (10.35 to 9.35001 MHz) through the low-pass filter and divide-by-10 counter to the phase/frequency discriminator. In the phase/frequency discriminator, the divide-by-10 output (1.035 to 0.935 MHz) is compared with the high reference input and produces an output control voltage.

The output control voltage is mixed with the tracking voltage input from the translator logic and vco circuits and applied to the output vco circuit. The output vco circuit receives the output control voltage signal from the output logic circuits and is driven to and locked at the variable injection frequency (109.35 to 79.3501 MHz).

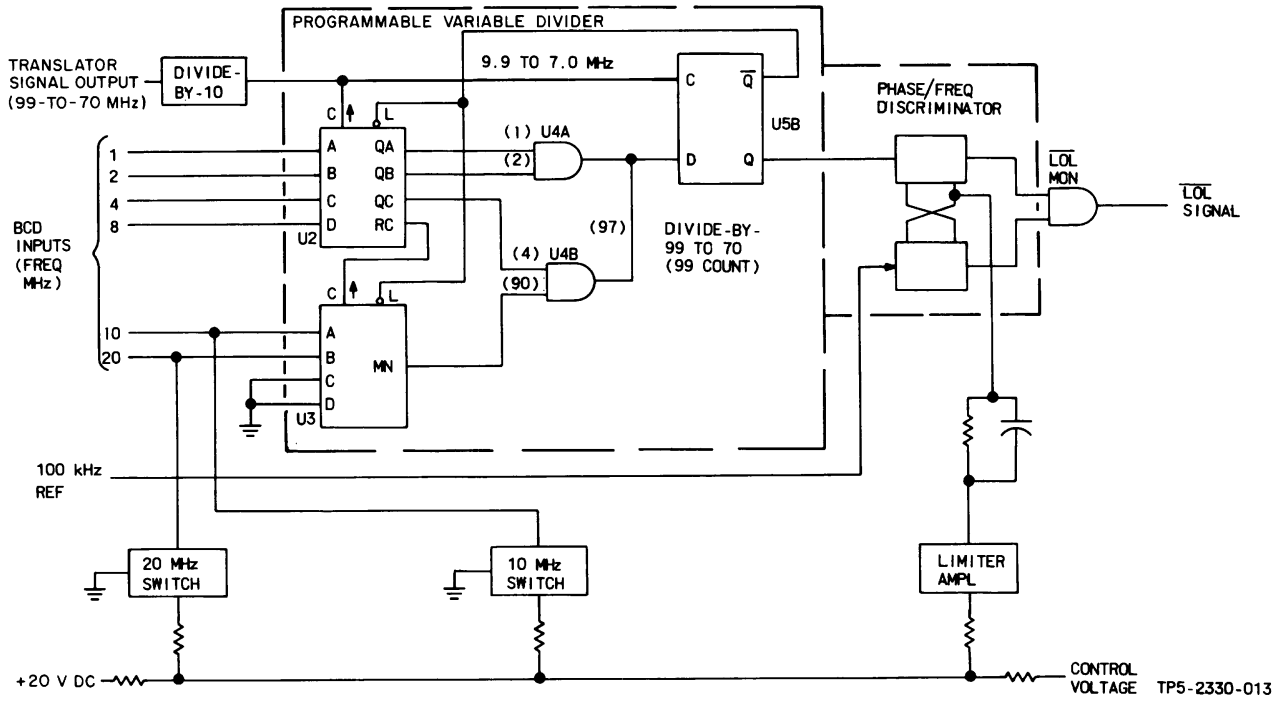
The output vco circuit is phase-locked to the high reference input and through the translator phase-lock loop to the 100-kHz reference input.

The output vco output (109.35 to 79.3501 MHz) is supplied as the variable injection to associated rf circuits.

2.2 Translator Logic Circuits

The translator logic circuits receive a 100-kHz reference input, a translator vco signal output, and bcd frequency inputs for 0, 1, 2, 4, 8, 10, and 20 MHz; it also supplies a control voltage output signal to the translator vco.

Refer to figure 3. The translator vco signal output (99 to 70 MHz) is supplied through a fixed divide-by-10 network (9.9 to 7.0 MHz) and applied as the clock input to a programmable variable divider. The output of the programmable variable divider (100 kHz) is supplied to a phase/frequency discriminator and is compared with a 100-kHz reference input. A phase or frequency difference in the discriminator causes a control voltage input increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output indicating the vco frequency is locked. Note that a 10- or 20-MHz bcd input enables switches that change the limiter amplifier voltage divider ratio to equalize the loop gain over the frequency range.



Translator Logic Circuits
Figure 3

The programmable variable divider is programmed by bcd frequency inputs. For example, if a bcd input of 00 MHz is applied, the up/down decade counter is programmed to load the count 0 at any time a load signal (logic 0) is applied. Refer to table 1. This programs the variable divider to count from 0 (first count 1) to 99 (last count 99/0), causing the output of the variable divider to be 1/99th of the clock input, or divide-by-99 with a bcd input of 00. Note that as the bcd input goes up 1, 2, 3 etc, the division ratio goes down 98, 97, 96, etc. Also note that for the divide-by circuit to operate as a constant, the last count 99 must also be the loaded count (in the case of bcd 00, count 0). To do this, prerecognition of count 99 is required. Look-ahead circuit of U4A and U4B performs this function. At clock 97 (count 97) gates U4A and U4B are ANDed and supply a logic 1 input to U5B-D. With a logic 1 at U5B-D, clock 98 (count 98) causes U5B-$\overline{Q}$ to go to logic 0 and loads decade counter to bcd input (ANDed outputs of U4A and U4B are removed). At clock 98, U5B-Q supplies a pulse to phase/frequency discriminator. Clock 99 (count 00) causes U5B-$\overline{Q}$ to go to logic 1 and enables decade counter to count on the next clock. Next clock is one above the bcd programmed input. Note that count 98 initiates the output from the divider and count 99 appears only as the bcd programmed input. Refer to figure 4. A 15-MHz programmed input is shown; the same principles apply to any other programmed bcd input.

2.3 Translator VCO Circuits

The translator vco circuits receive a control voltage from the translator logic circuits. The control voltage drives the vco to the required translator frequency. The translator signal output is supplied through one buffer amplifier to the output mixer circuits and through a second buffer amplifier to the translator logic circuits.

2.4 Output Mixer Circuits

The output mixer circuits receive a translator signal input (99 to 70 MHz) from the translator vco. The translator vco signal is mixed with the output vco frequency (109.35 to 79.35001 MHz) and a resulting difference frequency (10.35 to 9.35001 MHz) is supplied through a low-pass filter to the output logic circuits.

2.5 Output Logic Circuits

The output logic circuits receive the output mixer difference frequency (10.35 to 9.35001 MHz), a tracking voltage from the translator vco, and a high reference input signal (1.035 to 0.935001 MHz), and supply a control voltage output signal to operate the output vco.

Table 1. Variable Divider, Logic Truth Table.

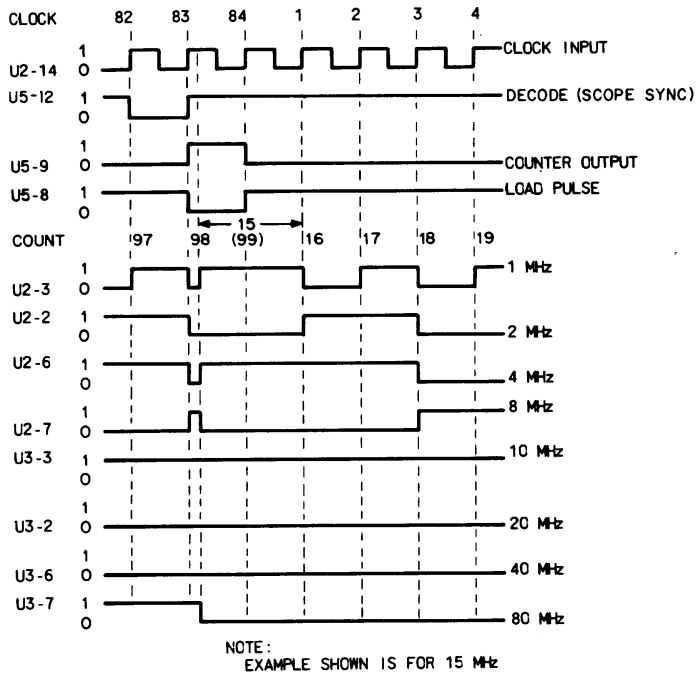
FREQUENCY CONTROL (MHz)	PROGRAMMABLE INPUTS								OUTPUT COUNT	DIVIDE-BY	LOOP FREQUENCY (MHz)
	U2				U3						
	A	B	C	D	A	B	*C	*D			
0	0	0	0	0	0	0	0	0	0	99	99
1	1	0	0	0	0	0	0	0	1	98	98
2	0	1	0	0	0	0	0	0	2	97	97
3	1	1	0	0	0	0	0	0	3	96	96
4	0	0	1	0	0	0	0	0	4	95	95
5	1	0	1	0	0	0	0	0	5	94	94
6	0	1	1	0	0	0	0	0	6	93	93
7	1	1	1	0	0	0	0	0	7	92	92
8	0	0	0	1	0	0	0	0	8	91	91
9	1	0	0	1	0	0	0	0	9	90	90
10	0	0	0	0	1	0	0	0	10	89	89
11	1	0	0	0	1	0	0	0	11	88	88
12	0	1	0	0	1	0	0	0	12	87	87
13	1	1	0	0	1	0	0	0	13	86	86
14	0	0	1	0	1	0	0	0	14	85	85
15	1	0	1	0	1	0	0	0	15	84	84
16	0	1	1	0	1	0	0	0	16	83	83
17	1	1	1	0	1	0	0	0	17	82	82
18	0	0	0	1	1	0	0	0	18	81	81
19	1	0	0	1	1	0	0	0	19	80	80
20	0	0	0	0	0	1	0	0	20	79	79
21	1	0	0	0	0	1	0	0	21	78	78
22	0	1	0	0	0	1	0	0	22	77	77
23	1	1	0	0	0	1	0	0	23	76	76
24	0	0	1	0	0	1	0	0	24	75	75
25	1	0	1	0	0	1	0	0	25	74	74
26	0	0	1	0	0	1	0	0	26	73	73
27	1	1	1	0	0	1	0	0	27	72	72
28	0	0	0	1	0	1	0	0	28	71	71
29	1	0	0	1	0	1	0	0	29	70	70

*Grounded inputs (fixed logic 0)

Refer to figure 5. The output mixer difference frequency (10.35 to 9.35001 MHz) is supplied through a squaring amplifier and a fixed divide-by-10 network (1.035 to 0.935001 MHz), to a phase/frequency discriminator. This frequency from the divide-by-10 network is compared with the high reference input signal (1.035 to 0.935001 MHz). A phase or frequency difference in the discriminator causes the control voltage to increase or decrease to adjust the frequency of the vco. If there is no phase or frequency difference, the discriminator provides a logic 1 lock signal output and the vco frequency locks. Note that the translator tracking voltage is summed with the output logic circuits' control voltage to provide control voltage for the total variable injection frequency output (109.35 to 79.35001 MHz).

2.6 Output VCO Circuits

The output vco circuits receive a control voltage from the output logic circuits. The control voltage drives the vco to the required output variable injection frequency. The output variable injection frequency is supplied through one output amplifier to the unit under control and through a second output amplifier to the output mixer circuits.



MHz	PROGRAMMED BCD INPUTS PIN NO.	LOGIC LEVEL
1	U2-15	1
2	U2-1	0
4	U2-10	1
8	U2-9	0
10	U3-15	1
20	U3-1	0
40	U3-10	FXD 0
80	U3-9	FXD 0

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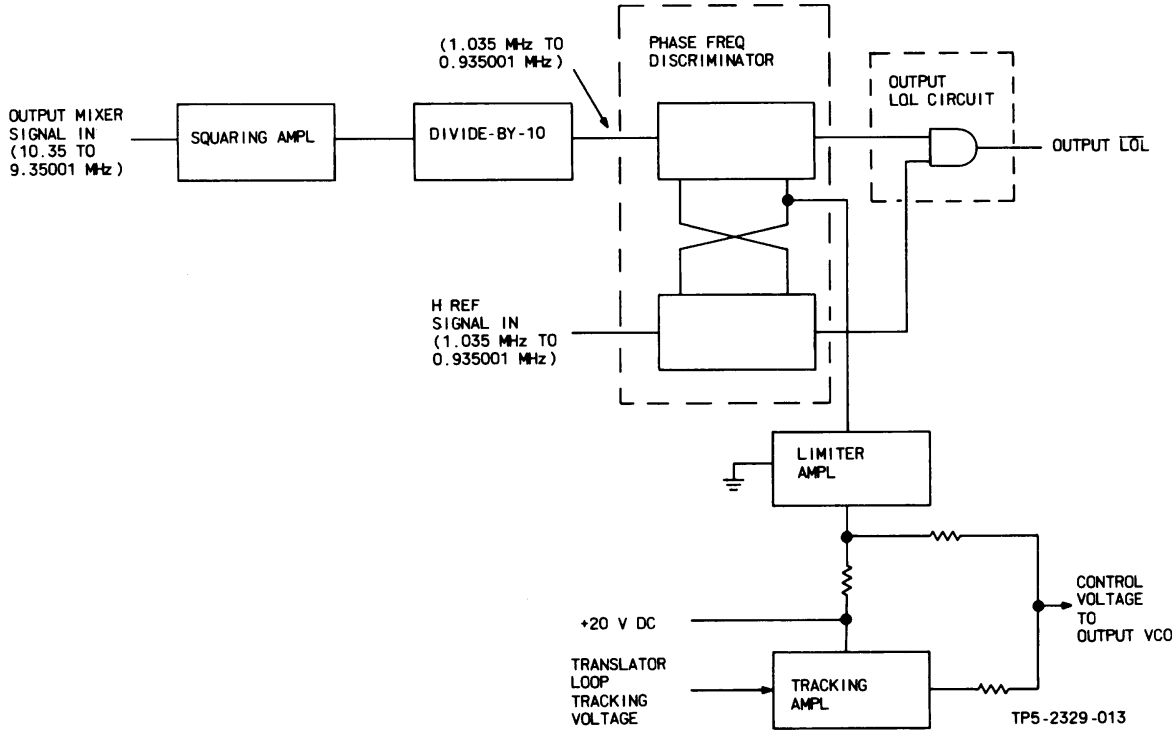
Variable Divider, Inputs and Outputs
Figure 4



Output Logic Circuits
Figure 5

2.7 Up/Down Decade Counter 74LS190 (Refer to table 2 and figure 6.)

The 74LS190 up/down decade counter is a 4-bit decade counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met.

A high at the enable input inhibits counting. A low at the enable input and a low-to-high clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is high. The down/up input determines the direction of the count. When low, the count goes up; when high, the count goes down.

These counters are programmable. The outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the state of the clock input. This allows the counters to be used as modulo N dividers by modifying the count length with the preset inputs.

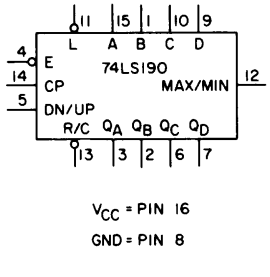
Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters are cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

2.8 Decade Counter 74LS90 (Refer to table 3 and figure 7.)

The 74LS90 decade counter is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-2 counter and a divide-by-5 counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logic 0 or to a binary coded decimal (bcd) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated into the three following independent count modes:

a. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the bcd count sequence truth table shown above. In addition to a conventional 0 reset, inputs are provided to reset a bcd 9-count for 9's complement decimal applications.

b. If a symmetrical divide-by-10 count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of 10, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-10 square wave is obtained at output A.



Up/Down Decade Counter 74LS190
Figure 6

Table 2. Up/Down Decade Counter, Logic Truth Table.

PROGRAMMABLE INPUTS				COUNT	BCD OUTPUTS			
A	B	C	D		QA	QB	QC	QD
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	2	0	1	0	0
1	1	0	0	3	1	1	0	0
0	0	1	0	4	0	0	1	0
1	0	1	0	5	1	0	1	0
0	1	1	0	6	0	1	1	0
1	1	1	0	7	1	1	1	0
0	0	0	1	8	0	0	0	1
1	0	0	1	9	1	0	0	1

E (enable): logic 0 enables counter; logic 1 inhibits counter.

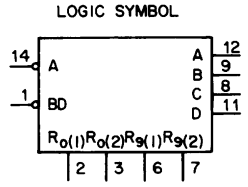
L (load): logic 0 programs the bcd output count to be set at the bcd count of the programmable inputs; the next clock pulse counts one higher/lower (up/down).

DU (down/up): logic 0 counts up; logic 1 counts down.

CP (clock pulse): logic 0-to-logic 1 transition advances counter.

RC (ripple clock): logic 0 pulse equal to 1/2 clock cycle when an overflow occurs.

MM (maximum/minimum count): logic 1 pulse equal to full clock cycle when an overflow or underflow occurs.



Decade Counter 74LS90
Figure 7

c. For operation as a divide-by-2 counter and divide-by-5 counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-2 function. The BD input is used to obtain binary divide-by-5 operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

2.9 Dual D-Type Flip-Flop With Preset and Clear 74LS74 (Refer to table 4 and figure 8.)

The 74LS74 consists of dual high-speed, D-type flip-flops. Information on the D input is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either high or low level, the D input signal has no effect.

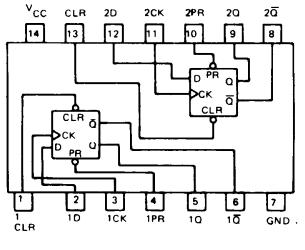
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the synthesizer output module are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 5 check total performance of the synthesizer output module. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



Dual D-Type Flip-Flop With Preset and Clear 74LS74
Figure 8

Table 3. Decade Counter 74LS90, Logic Truth Table.

*BCD COUNT SEQUENCE				
COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

**RESET/COUNT							
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	Count			
0	X	0	X	Count			
0	X	X	0	Count			
X	0	0	X	Count			

*Output A connected to input BD for BCD count.
**X indicates that either a logical 1 or a logical 0 may be present.

Table 4. Dual D-Type Flip-Flop With Preset and Clear 74LS74, Logic Truth Table.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	*H	*H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Table 5. Synthesizer Output, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of the unit containing the synthesizer output that is to be tested.		
	b. Remove cover from the synthesizer section of the unit.		
	c. Remove synthesizer output and install it on an extender card and place it in the unit.		
	d. Set unit LINE SELECTOR switch to 115 V.		
	e. Connect unit to 115-V ac power source and set power on.		
	f. Measure dc voltage from J1-19 to J1-17 (ground).	+5.2 ±0.2 V dc.	Check unit synthesizer voltage regulator.
	g. Measure dc voltage from J1-7 to J1-17 (ground).	NLT +19.5 V dc. NMT +20.8 V dc.	Check unit synthesizer voltage regulator.
	h. Measure dc voltage from J1-20 to J1-17 (ground).	+8.0 ±0.5 V dc.	Check unit power supply.
	i. Set unit MODE switch to ISB.		
2. Synthesizer output	a. Set FREQUENCY KHZ control on front panel to 29555.55 (or 29555.5).		
	b. Using a frequency counter, measure the high reference input between P1-1 and P1-2 (ground).	979 ±1 kHz. Note actual frequency	Check unit decades one at a time.
	c. Measure the dc voltage at A3E110. (Refer to note and chart at end of test 2 for voltages and frequencies at different 10 and 1 MHz settings.)	4.51 ±0.1 V dc.	Adjust L2 for 4.90 ±0.1 V dc. If L2 adjustment does not correct the problem check Q4, Q5, and associated circuit.
	d. Using a frequency counter, measure the output at P2.	79.79 ±0.005 MHz. (Actual should equal 79.35 MHz plus the difference between 1035 kHz and the actual frequency in step a.)	Adjust L3 for actual frequency with required V dc at A1E100. If L3 adjustment does not correct the problem check A1A1Q1, A1A1Q2, A1A103, and associated circuits.
	e. Measure the dc voltage at A1E100.	4.80 ±0.1 V dc.	Same as step d.
	f. Note the dc voltage at A1E100 while moving the 10 and 1 MHz frequency controls from 9 down to 0.	Refer to chart at end of test 2. (Voltage goes up as frequency controls go down.)	Adjust L3 so that all settings fall into the limits shown in chart.
(Cont)			

Table 5. Synthesizer Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	g. Set FREQUENCY KHZ control on front panel to 00000.00 (or 00000.0).		
	h. Using a frequency counter, measure the high reference input between P1-1 and P1-2 (ground).	1035 ±0.5 kHz.	Check unit 100-kHz decade.
	i. Using a frequency counter, measure the output at P2.	109.350 MHz ±0.5 kHz.	Check A4A1U1 thru A4A1U5 and associated circuits.
	j. Set FREQUENCY KHZ control on front panel to 29999.99 (or 29999.9).		
	k. Using a frequency counter, measure the output at P2.	79.350 MHz ±0.5 kHz.	Same as step i.
	l. Measure the dc voltage at P1-8 to ground.	NLT +3.5 V dc. **Note** RCV FAULT, EXCTR FAULT, or R/E FAULT indicator lighting indicates that results of step m are satisfactory.	Check A4A1U4 and A4A1U6 thru A4A1U8.
	m. Ground P1-10 while noting the voltage at P1-8.	NMT 0.5 V dc.	Same as step l.
	n. Remove P1-10 ground.		
	o. Set front-panel PWR switch off.		
	p. Remove 100-kHz decade from unit under test.		
	q. Set front-panel PWR switch on.		
	r. Measure the dc voltage at P1-8 to ground.	NMT 0.5 V dc.	Check A2A1U3 thru A2A1U5.
	s. Set front-panel PWR switch off.		
(Cont)	t. Replace 100-kHz decade in unit under test.		

Table 5. Synthesizer Output, Testing and Troubleshooting Procedures (Cont).

TEST	PROCECURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

2. (Cont)

Note

The following chart is shown with an input frequency of 1035 ±5 kHz. The actual output frequency with an input frequency can be determined using the following formula:

AF = LF - 100 kHz + 1035 kHz - IF.

AF = actual output frequency at P1-1.

LF = output frequency listed in chart for associated MHz frequency digits.

IF = actual input frequency.

10-MHz FREQ DIGIT	1-MHz FREQ DIGIT	A3E110 DC VOLTAGE	XLTR FREQ A3A1E9 (MHz)	A1E100 DC VOLTAGE	OUTPUT FREQ P2 (MHz)
2	9	4.90	70.000	4.80	80.350
	8	5.20	71.000	5.05	81.350
	7	5.50	72.000	5.30	82.350
	6	5.80	73.000	5.60	83.350
	5	6.10	74.000	5.85	84.350
	4	6.40	75.000	6.15	85.350
	3	6.70	76.000	6.40	86.350
	2	7.05	77.000	6.70	87.350
	1	7.35	78.000	7.00	88.350
	0	7.70	79.000	7.25	89.350
1	9	8.00	80.000	7.55	90.350
	8	8.35	81.000	7.85	91.350
	7	8.70	82.000	8.15	92.350
	6	9.00	83.000	8.45	93.350
	5	9.35	84.000	8.80	94.350
	4	9.70	85.000	9.10	95.350
	3	10.10	86.000	9.40	96.350
	2	10.45	87.000	9.75	97.350
	1	10.85	88.000	10.05	98.350
	0	11.20	89.000	10.40	99.350
0	9	11.60	90.000	10.75	100.350
	8	12.00	91.000	11.10	101.350
	7	12.40	92.000	11.50	102.350
	6	12.85	93.000	11.90	103.350
	5	13.30	94.000	12.30	104.350
	4	13.75	95.000	12.75	105.350
	3	14.20	96.000	13.25	106.350
	2	14.70	97.000	13.75	107.350
	1	15.25	98.000	14.30	108.350
	0	15.80	99.000	14.90	109.350

Note

Table shown with an input frequency of 1035 ±5 kHz (front-panel FREQUENCY KHZ setting of XX000.00 (or XX000.0)). Frequencies shown ±0.0005 MHz, voltages shown ±0.1 V dc.

4. ALIGNMENT/ADJUSTMENT

Note

Perform these adjustments only if repairs have been made and test procedures in table 5 cannot meet the normal indications.

4.1 Translator VCO Tracking

a. Perform setup of table 5, test 1.
b. Adjust the slug in oscillator coil A3A1L2 to approximately 1.6 mm (1/16 in) below coil form.
c. Adjust the plates in oscillator capacitor A3A1C7 two turns below the top of capacitor form.
d. Set front-panel FREQUENCY KHZ to 29000.00 (or 29000.0).
e. Connect a frequency counter between P1-1 and P1-2 (ground). Must equal 1035 ±0.5 kHz.
f. Connect a frequency counter between P1-10 and P1-9 (ground). Must equal 100 ±0.01 kHz.
g. Connect a frequency counter at A3A1E5 to A3A1E4 (ground).
h. Adjust the slug in oscillator coil A3A1L2 for 70.000 MHz ±20 kHz.
i. Set front-panel FREQUENCY KHZ to 00000.00 (or 00000.0).
j. Adjust the plates in oscillator capacitor A3A1C7 for 99.000 MHz ±20 kHz.

Note

Adjust capacitor A3A1C7 for an error opposite the error of coil A3A1L2. Example, if A3A1L2 is adjusted at 70.000 MHz minus 20 kHz, adjust A3A1C7 for 99.000 MHz plus 20 kHz.

k. Repeat steps f through j until low and high frequencies are within 10 kHz of the correct frequency.

4.2 Output VCO Tracking

a. Perform setup of table 5, test 1.
b. Adjust the slug in oscillator coil A1A1L3 to approximately 1.6 mm (1/16 in) below coil form.
c. Adjust the plates in oscillator capacitor A1A1C2 two turns below the top of capacitor form.
d. Set front-panel FREQUENCY KHZ to 29000.00 (or 29000.0).
e. Connect a frequency counter between P1-1 and P1-2 (ground). Must equal 1035 ±0.5 kHz.
f. Connect a frequency counter between P1-10 and P1-9 (ground). Must equal 100 ±0.01 kHz.
g. Connect a frequency counter with 50-Ω load at P2.
h. Adjust the slug in oscillator coil A1A1L3 for 80.350 MHz ±20 kHz.
i. Set front-panel FREQUENCY KHZ to 00000.00 (or 00000.0).
j. Adjust the plates in oscillator capacitor A1A1C2 for 109.350 MHz ±20 kHz.

Note

Adjust capacitor A1A1C2 for an error opposite the error of coil A1A1L3. Example, if A1A1L3 is adjusted at 80.350 MHz minus 20 kHz, adjust A1A1C2 for 109.350 MHz plus 20 kHz.

k. Repeat steps f through j until low and high frequencies are within 10 kHz of the correct frequency.

4.3 Output VCO Level Adjustment

a. Perform setup of table 5, test 1.
b. Connect an rf voltmeter with 50-Ω load to P2.
c. Set front-panel FREQUENCY KHZ to 16000.00 (or 16000.0).
d. Adjust A1A1R4 for +7 dB mW on rf voltmeter.

Note

A1A1R10 may be replaced with a selected resistor (50 through 720 Ω) to meet this adjustment.

4.4 Output VCO Final Tuning

a. Perform setup of table 5, test 1.
b. Connect a high-impedance scope probe to A2A1U4-6.

Note

A steady rectangular waveform should be seen. The object of this adjustment is to make the rectangular waveform as near a square wave as possible throughout the synthesizer output tuning range.

c. Set front-panel FREQUENCY KHZ controls to 29 555.55 kHz.
d. Adjust A1A1L3 for a 42-percent duty ratio (square wave, 42-percent logic 1, 58-percent logic 0).
e. Set front-panel FREQUENCY KHZ controls to 00 555.55 kHz.

f. Adjust A1A1C2 for duty ratio, opposite that indicated. For example, if a 30-percent duty ratio is indicated, adjust for a 70-percent duty ratio.
g. Repeat steps c through f until the duty ratio at both end frequencies is between 45 and 55 percent.

5. REPAIR

Repair of the synthesizer output module is accomplished using standard planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

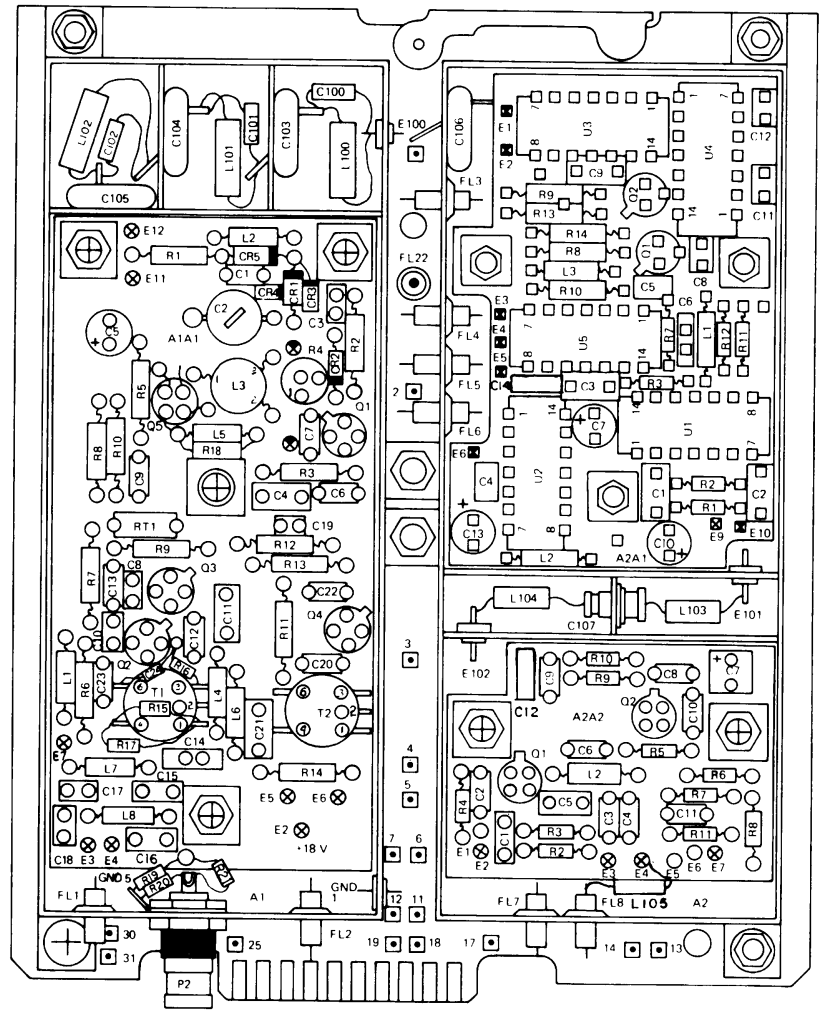
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram (figure 9). The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description is listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses, and on the schematic diagram inside an arrow that points at the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Synthesizer output	635-4930-001	REV E
Output vco assy A1	637-1760-001	REV E
Output vco board A1A1	635-0890-002	REV F
Output mixer-logic assy A2	637-1761-001	REV E
Output logic board A2A1	635-0836-001	REV C
Output mixer board A2A2	635-0837-001	REV B
Translator vco assy A3	637-1763-001	REV F
Translator vco board	635-0846-001	REV D
Translator logic assy A4	637-1762-001	REV D
Translator logic board	635-0646-001	REV B



TP5-1230-019

Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 1 of 5)

PARTS LIST

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
	SYNTH OUTPUT 635-4930-001		
A1	OUTPUT VCO	637-1760-001	
A2	OUTPUT MIXER/LOGIC	637-1761-001	
A3	TRANSLATOR VCO	637-1763-001	
A4	TRANSLATOR LOGIC	637-1762-001	
A5	CONNECTOR BOARD	635-0998-001	
FL1-FL21	NOT USED		
FL22	FILTER, RAD INTR 1750pF	241-5006-010	
	OUTPUT VCO A1 637-1760-001		
A1	OUTPUT VCO BOARD	635-0890-002	
C1-C99	NOT USED		
C100	CAPACITOR, FXD, CER DIEL, 18pF, 10%, 75V	913-1098-030	
C101	CAPACITOR, FXD, CER DIEL, 0.00015μF, 5%, 100V	913-3117-050	
C102	CAPACITOR, FXD, MICA DIEL, 68pF, ±0.5pF, 50V	912-4141-330	
C103, C104	CAPACITOR, FXD, MICA DIEL, 1500pF, 5%, 500V	912-4114-370	
C105	CAPACITOR, FXD, MICA DIEL, 750pF, 5%, 500V (A8)	912-4114-350	
C105	CAPACITOR, FXD, MICA DIEL, 1500pF, 5%, 500V	912-4114-370	
FL1, FL2	FILTER, RAD INTR, 1750pF	241-5006-010	
L1-L99	NOT USED		
L100-L102	COIL, RF, 15000μH	240-2715-630	
P1	NOT USED		
P2	CONNECTOR, RCPT, ELEC	357-7207-090	
R1-R18	NOT USED		
R19, R20	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/8W (A7)	745-2320-000	
R21	RESISTOR, FXD, CMPSN, 18Ω, 10%, 1/8W (A7)	745 2277-000	
	OUTPUT VCO BOARD A1A1 635-0890-002		
CR1	SEMICOND DEVICE, BB109	922-6131-010	
CR2	SEMICOND DEVICE, 1N5711	353-3691-010	
CR3-CR5	SEMICOND DEVICE, BB109 (A6)	922-6131-010	
C1	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V (A6)	913-4018-000	
C2	CAPACITOR, VAR, AIR DIEL, 1 TO 10pF, 200V	922-0583-230	
C3	CAPACITOR, FXD, CER DIEL, 18pF, 10%, 75V	913-1098-030	
C4	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C5	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C6	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V (A6)	913-4018-000	
C6	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C7	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C8	CAPACITOR, FXD, CER DIEL, 15pF, 5%, 75V (A6)	913-1098-180	
C9	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V (A6)	913-4018-000	
C9	CAPACITOR, FXD, MICA DIEL, 27pF, 5%, 50V	912-4141-180	
C10	CAPACITOR, FXD, CER DIEL, 0.00047μF, 5%, 100V	913-3117-080	
C11	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C12, C13	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C14	CAPACITOR, FXD, CER DIEL, 47pF, ±0.25pF, 150V	913-1098-370	
C15	CAPACITOR, FXD, MICA DIEL, 33pF, 5%, 50V	913-4141-220	
C16	CAPACITOR, FXD, MICA DIEL, 51pF, 5%, 50V	912-4141-300	
C17	CAPACITOR, FXD, CER DIEL, 0.00068μF, 5%, 100V	913-3117-090	
C18	CAPACITOR, FXD, CER DIEL, 270pF, 5%, 100V	913-1098-470	
C19	CAPACITOR, FXD, CER DIEL, 3pF, ±0.25pF, 150V	913-1098-340	
C20	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C21	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C22	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C23	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C24	CAPACITOR, FXD, MICA DIEL, 8pF, ±.5pF, 300V (A6)	912-4141-110	
L1	COIL, RF, 100μH	240-2047-000	
L2	COIL, RF, 2.70μH (A6)	240-2028-000	
L2	COIL, RF, 15μH	240-2037-000	
L3	COIL, ADJUSTABLE	637-4502-001	
L4	COIL, RF, 100μH	240-2047-000	
L5	COIL, RF, 1μH (A4)	240-2023-000	
L6	COIL, RF, 100μH	240-2047-000	

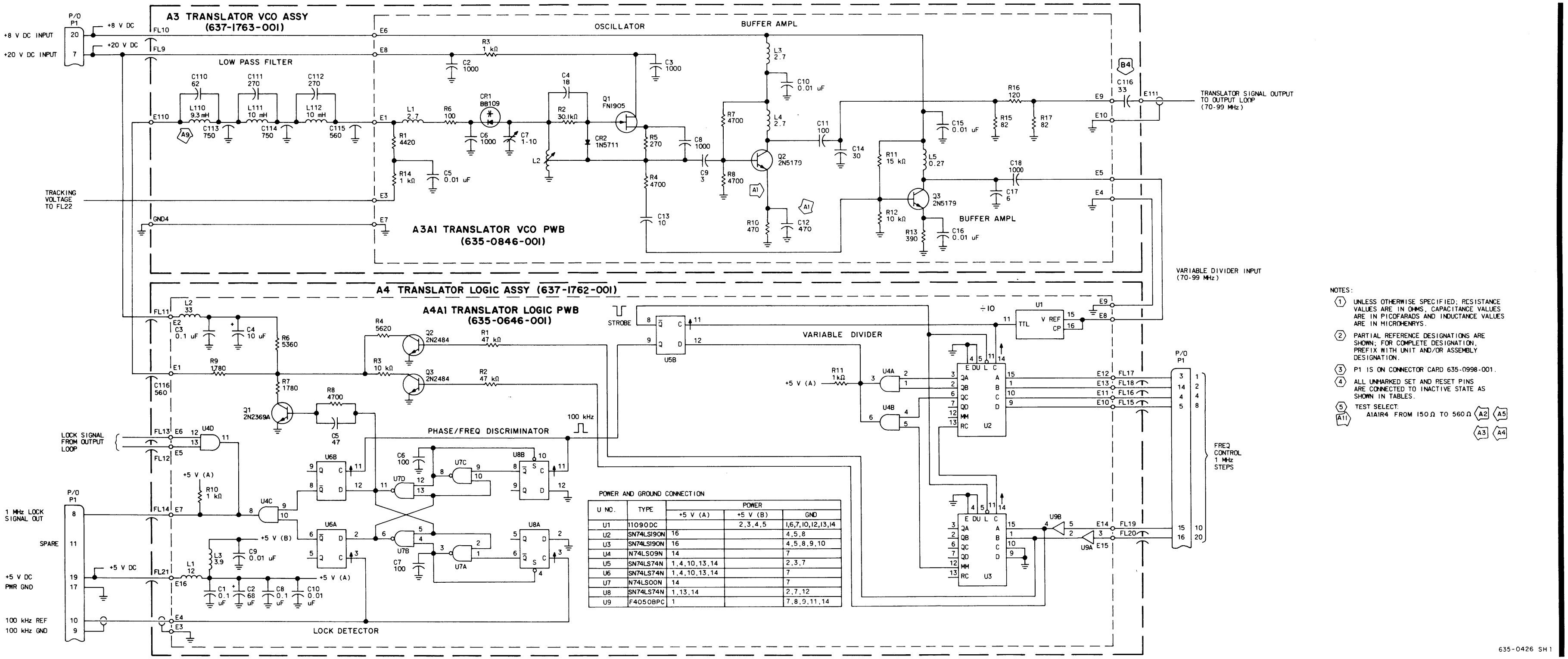
PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART	USABLE ON CODE
L7, L8	COIL, RF, 0.100μH	240-2723-140	
Q1	TRANSISTOR, FN1905	352-0756-050	
Q2	TRANSISTOR, 2N918	352-0440-000	
Q3, Q4	TRANSISTOR, 2N5179	352-0792-020	
Q5	TRANSISTOR, FN1905 (A5)	352-0756-050	
R1	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R2	RESISTOR, FXD, FILM, 30.1kΩ, 1%, 1/8W (A6)	705-1067-000	
R2	RESISTOR, FXD, FILM, 68.1kΩ, 1%, 1.8W	705-1084-000	
R3	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W (A6)	745-0749-000	
R3	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R4	RESISTOR, VAR, 1kΩ, 10%, 0.5W (A11)	382-00	
R4	RESISTOR, FXD, CMPSN, 150 THRU 560Ω, 10%, 1/4W	638-6457-001	
R5	RESISTOR, FXD, CMPSN, 220Ω, 10%, 1/4W	745-0725-000	
R6	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R7	RESISTOR, FXD, CMPSN, 1.5kΩ, 10%, 1/4W	745-0755-000	
R8	RESISTOR, FXD, CMPSN, 2.2kΩ, 10%, 1/4W	745-0761-000	
R9	RESISTOR, FXD, CMPSN, 68Ω, 10%, 1/4W (A5)	745-0707-000	
R9	RESISTOR, FXD, CMPSN, 22Ω, 10%, 1/4W	745-0689-000	
R10	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W (A2)	745-0713-000	
R10	RESISTOR, FXD, CMPSN, 100 THRU 390Ω, 10%, 1/4W (A5)	638-1088-001	
R10	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/4W	745-0722-000	
R11	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/4W	745-0764-000	
R12	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/4W (A2)	745-0743-000	
R12	RESISTOR, FXD, CMPSN, 560Ω, 10%, 1/4W	745-0740-000	
R13	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R14	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/4W	745-0704-000	
R15	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/8W (A3, A4) OR	745-2304-000	
R15	RESISTOR, FXD, CMPSN, 150Ω, 10%, 1/8W (A3, A4)	745-2311-000	
R16	RESISTOR, FXD, CMPSN, 47Ω, 10%, 1/8W (A6)	745-2292-000	
R17	RESISTOR, FXD, CMPSN, 330Ω, 10%, 1/8W (A6)	745-2323-000	
R18	RESISTOR, FXD, CMPSN, 820Ω, 10%, 1/8W (A6)	745-2338-000	
RT1	RESISTOR, THRM, 220Ω, 10%, 1/2W	714-1721-000	
T1	TRANSFORMER, RF (A5)	278-0430-200	
T1	TRANSFORMER, RF	278-0430-290	
T2	TRANSFORMER, RF	278-0430-200	
	OUTPUT MIXER/LOGIC A2 637-1761-001		
A1	OUTPUT LOGIC BOARD	635-0836-001	
A2	OUTPUT MIXER BOARD	635-0837-001	
C1-C105	NOT USED		
C106	CAPACITOR, FXD, MICA DIEL, 750pF, 5%, 500V	912-4114-350	
C107	CAPACITOR, FXD, CER DIEL, 15pF, 20%, 500V	913-3111-050	
FL1, FL2	NOT USED		
FL3-FL8	FILTER, RAD INTR, 1750pF	241-5006-010	
L1-L102	NOT USED		
L103-L104	COIL, RF, 10μH	240-2715-250	
L105	COIL, RF, 100μH (B3)	240-2047-000	
	OUTPUT LOGIC BOARD A2A1 635-0836-001		
C1-C3	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C4	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C5	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C6	CAPACITOR, FXD, CER DIEL, 47pF, 10%, 75V	913-1098-020	
C7	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-680	
C8	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
C9	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-200	
C10	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C11, C12	CAPACITOR, FXD, CER DIEL, 100pF, 5%, 100V	913-3281-280	
C13	CAPACITOR, FXD, ELCTLT, 0.47μF, 20%, 35V	184-9102-330	
C14	CAPACITOR, FXD, MICA DIEL, 150pF, 5%, 50V (B2)	912-4141-400	
L1, L2	COIL, RF, 100μH	240-2047-000	
L3	COIL, RF, 4.70μH (B2)	240-2031-000	
L3	COIL, RF, 100μH	240-2047-000	
Q1	TRANSISTOR, 2N930	352-0517-010	
Q2	TRANSISTOR, 2N2369A	352-0596-030	
R1, R2	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/8W	745-2329-000	

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
R3	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-2341-000	
R4-R6	NOT USED		
R7	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R8	RESISTOR, FXD, FILM, 33.2kΩ, 1%, 1/8W (A10)	705-1069-000	
R8	RESISTOR, FXD, FILM, 21kΩ, 1%, 1/8W	705-3605-630	
R9	RESISTOR, FXD, FILM, 3.48kΩ, 1%, 1/8W	705-1022-000	
R10	RESISTOR, FXD, FILM, 3.83kΩ, 1%, 1/8W	705-1024-000	
R11	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/20W	705-3163-120	
R12	RESISTOR, FXD, CMPSN, 10Ω, 10%, 1/8W	745-2377-000	
R13	RESISTOR, FXD, FILM, 4.64kΩ, 1%, 1/8W	705-1028-000	
R14	RESISTOR, FXD, FILM, 464Ω, 1%, 1/8W	705-0980-000	
U1	INTEGRATED CKT, N74LS04N	351-1523-090	
U2	INTEGRATED CKT, SN74LS90N	351-1636-010	
U3	INTEGRATED CKT, SN74LS74N	351-1525-040	
U4	INTEGRATED CKT, N74LS00N	351-1523-110	
U5	INTEGRATED CKT, SN74LS74N	351-1525-040	
	OUTPUT MIXER BOARD A2A2 635-0837-001		
C1	CAPACITOR, FXD, MICA DIEL, 10pF, ±0.5pF, 50V	912-4141-020	
C2, C3	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	912-4018-000	
C4	CAPACITOR, FXD, CER DIEL, 0.1μF, 10%, 50V	913-5019-320	
C5	CAPACITOR, FXD, MICA DIEL, 5pF, ±0.5pF, 50V	912-4141-010	
C6	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C7	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C8-C10	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C11	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C12	CAPACITOR, FXD, MICA DIEL, 22pF ±0.5pF, 300V (B1)	912-4141-030	
L1	NOT USED		
L2	COIL, RF, 0.18μH	240-2014-000	
Q1	TRANSISTOR, 2N5179	352-0792-020	
Q2	TRANSISTOR, 3N187	352-1093-010	
R1	NOT USED		
R2	RESISTOR, FXD, CMPSN, 2.7kΩ, 10%, 1/8W	745-2356-000	
R3	RESISTOR, FXD, CMPSN, 680Ω, 10%, 1/8W	745-2335-000	
R4	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/8W	745-2304-000	
R5	RESISTOR, FXD, CMPSN, 200Ω, 10%, 1/8W	745-2317-000	
R6	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/8W	745-2304-000	
R7	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/8W	745-2377-000	
R8	RESISTOR, FXD, CMPSN, 180Ω, 10%, 1/8W	745-2314-000	
R9, R10	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-2341-000	
R11	RESISTOR, FXD, CMPSN, 56Ω, 10%, 1/8W	745-2295-000	
	TRANSLATOR VCO A3 637-1763-001		
A1	TRANSLATOR VCO BOARD	635-0846-001	
C1-C109	NOT USED		
C110	CAPACITOR, FXD, MICA DIEL, 62pF, 5%, 50V	912-4141-320	
C111,C112	CAPACITOR, FXD, CER DIEL, 270pF, 5%, 100V	913-1098-470	
C113, C114	CAPACITOR, FXD, MICA DIEL, 750pF, 5%, 500V	912-4114-350	
C115	CAPACITOR, FXD, MICA DIEL, 560pF, 5%, 500V	912-4114-320	
C116	CAPACITOR, FXD, MICA DIEL, 33pF, 2%, 50V (B4)	912-4141-220	
FL1-FL8	NOT USED		
FL9-FL10	FILTER, RAD INTR, 1750pF	241-5006-010	
L1-L109	NOT USED		
L110	COIL, RF, 10000μH (A9)	240-2715-610	
L110	COIL, WW, 9.3MH	634-5339-001	
L111, L112	COIL, RF, 10000μH	240-2715-610	
	TRANSLATOR VCO BOARD A3A1 635-0846-001		
CR1	SEMICOND DEVICE, BB109	922-6131-010	
CR2	SEMICOND DEVICE, 1N5711	353-3691-010	
C1	NOT USED		
C2, C3	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C4	CAPACITOR, FXD, CER DIEL, 18pF, 10%, 75V	913-1098-030	
C5	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C6	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
C7	CAPACITOR, VAR, AIR DIEL, 1 TO 10pF, 200V	922-0583-230	
C8	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	

Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 2)



POWER AND GROUND CONNECTION

U NO.	TYPE	POWER		
		+5 V (A)	+5 V (B)	GND
U1	11090DC		2,3,4,5	1,6,7,10,12,13,14
U2	SN74LS190N	16		4,5,8
U3	SN74LS190N	16		4,5,8,9,10
U4	N74LS09N	14		7
U5	SN74LS74N	1,4,10,13,14		2,3,7
U6	SN74LS74N	1,4,10,13,14		7
U7	N74LS00N	14		7
U8	SN74LS74N	1,13,14		2,7,12
U9	F4050BPC	1		7,8,9,11,14

NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN PICOFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. P1 IS ON CONNECTOR CARD 635-0998-001.
4. ALL UNMARKED SET AND RESET PINS ARE CONNECTED TO INACTIVE STATE AS SHOWN IN TABLES.
5. TEST SELECT A1A1R4 FROM 150 Ω TO 560 Ω (A1) (A2) (A5) (A3) (A4)

635-0426 SH 1

Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 3)

PARTS LIST (Cont)

REF DES	DESCRIPTION	COLLINS PART NO	USABLE ON CODE
C9	CAPACITOR, FXD, MICA DIEL, 3pF, ±0.5pF, 50V	912-4141-070	
C10	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C11	CAPACITOR, FXD, CER DIEL, 100pF, 5%, 100V	913-3281-280	
C12	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V (A1)	913-5019-200	
C12	CAPACITOR, FXD, CER DIEL, 470pF, 10%, 200V	913-4014-000	
C13	CAPACITOR, FXD, CER DIEL, 10pF, 5%, 75V	913-1098-010	
C14	CAPACITOR, FXD, MICA DIEL, 30pF, 5%, 50V	912-4141-200	
C15, C16	CAPACITOR, FXD, CER DIEL, 0.01μF, 10%, 100V	913-5019-200	
C17	CAPACITOR, FXD, MICA DIEL, 6pF, ±0.5pF, 50V	912-4141-090	
C18	CAPACITOR, FXD, CER DIEL, 1000pF, 10%, 200V	913-4018-000	
L1	COIL, RF, 2.70μH	240-2028-000	
L2	COIL, ADJUSTABLE	835-9660-001	
L3, L4	COIL, RF, 2.70μH	240-2028-000	
L5	COIL, RF, 0.27μH	240-2016-000	
Q1	TRANSISTOR, FN1905	352-0756-050	
Q2, Q3	TRANSISTOR, 2N5179	352-0792-020	
R1	RESISTOR, FXD, FILM, 4.42kΩ, 1%, 1/8W	705-1027-000	
R2	RESISTOR, FXD, FILM, 30.1kΩ, 1%, 1/8W	705-1067-000	
R3	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R4	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R5	RESISTOR, FXD, CMPSN, 270Ω, 10%, 1/4W	745-0728-000	
R6	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W	745-0713-000	
R7, R8	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/4W	745-0773-000	
R9	RESISTOR, FXD, CMPSN, 100Ω, 10%, 1/4W (A1)	745-0713-000	
R10	RESISTOR, FXD, CMPSN, 470Ω, 10%, 1/4W	745-0737-000	
R11	RESISTOR, FXD, CMPSN, 15kΩ, 10%, 1/4W	745-0791-000	
R12	RESISTOR, FXD, CMPSN, 10kΩ, 10%, 1/4W	745-0785-000	
R13	RESISTOR, FXD, CMPSN, 390Ω, 10%, 1/4W	745-0734-000	
R14	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/4W	745-0749-000	
R15	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W	745-0710-000	
R16	RESISTOR, FXD, CMPSN, 120Ω, 10%, 1/4W	745-0716-000	
R17	RESISTOR, FXD, CMPSN, 82Ω, 10%, 1/4W	745-0710-000	
	TRANSLATOR LOGIC A4 637-1762-001		
A1	TRANSLATOR LOGIC BOARD	635-0646-001	
C1-C115	NOT USED		
C116	CAPACITOR, FXD, MICA DIEL, 560pF, 5%, 500V	912-4114-320	
FL1-FL10	NOT USED		
FL11-FL21	FILTER, RAD IN TR, 1750pF	241-5006-010	
	TRANSLATOR LOGIC BOARD A4A1 635-0646-001		
C1	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-180	
C2	CAPACITOR, FXD, ELCTLT, 68μF, 20%, 6V	184-9102-040	
C3	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-180	
C4	CAPACITOR, FXD, ELCTLT, 10μF, 20%, 25V	184-9102-240	
C5	CAPACITOR, FXD, CER DIEL, 47pF, 10%, 75V	913-1098-020	
C6, C7	CAPACITOR, FXD, CER DIEL, 100pF, 5%, 100V	913-3281-280	
C8	CAPACITOR, FXD, CER DIEL, 0.1μF, 20%, 50V	913-3279-180	
C9, C10	CAPACITOR, FXD, CER DIEL, 0.01μF, 20%, 50V	913-3279-110	
L1	COIL, RF, 12μH	240-2036-000	
L2	COIL, RF, 33μH	240-2041-000	
L3	COIL, RF, 3.90μH	240-2030-000	
Q1	TRANSISTOR, 2N2369A	352-0596-030	
Q2, Q3	TRANSISTOR, 2N2484	352-0549-000	
R1, R2	RESISTOR, FXD, CMPSN, 47kΩ, 10%, 1/8W	745-2401-000	
R3	RESISTOR, FXD, FILM, 10kΩ, 1%, 1/8W	705-1044-000	
R4	RESISTOR, FXD, FILM, 5.62kΩ, 1%, 1/8W	705-1032-000	
R5	NOT USED		
R6	RESISTOR, FXD, FILM, 5.36kΩ, 1%, 1/8W	705-1031-000	
R7	RESISTOR, FXD, FILM, 1.78kΩ, 1%, 1/8W	705-1008-000	
R8	RESISTOR, FXD, CMPSN, 4.7kΩ, 10%, 1/8W	745-2365-000	
R9	RESISTOR, FXD, FILM, 1.78kΩ, 1%, 1/8W	705-1008-000	
R10, R11	RESISTOR, FXD, CMPSN, 1kΩ, 10%, 1/8W	745-0749-000	
U1	INTEGRATED CKT, 11C90DC	351-1653-020	
U2, U3	INTEGRATED CKT, SN74LS190N	351-1527-040	
U4	INTEGRATED CKT, N74LS09N	351-1523-210	
U5, U6	INTEGRATED CKT, SN74LS74N	351-1525-040	
U7	INTEGRATED CKT, N74LS00N	351-1523-110	
U8	INTEGRATED CKT, SN74LS74N	351-1525-040	
U9	INTEGRATED CKT, F4050BPC	351-8159-220	

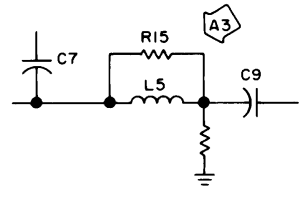
MODIFICATION HISTORY

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	Removed A3A1R9, 100Ω from in series with A3A1Q2-E and junction of A3A1R10-A3A1C12. Changed A3A1 C12 from 0.01μF to 470pF.	635-0846-001, REV B and above.
A2	Changed: A1A1R12 from 680u to 560u. A1A1R10 from 100u to test select of 100u to 390u.	635-0890-002, REV A and above.
A3	Added A1A1R15, test select of 100u or 150u.	635-0890-002, REV C and above.
A4	Removed A1A1L5, 1μH and A1A1R15, test select of 100u or 150u from circuit as shown below.	635-0890-002, REV E and above.
A5	Added A1A1 Q5, FN1905 Changed: A1A1R9 from 68Ω to 22Ω A1A1R10 from test select of 100Ω to 390Ω; to 180Ω fixed. A1A1T1 changed from 278-0430-200 to 278-0430-290.	635-0890-002, REV E and above.

A6	Removed A1A1C1, 1000pF from A1A1CR1 cathode to ground.
	Removed A1A1C8, 15pF from A1A1Q3-B to ground.
	Changed:
	A1A1C6 from 1000pF to 470pF
	A1A1C9 from 1000pF to 27pF
	A1A1L2 from 2.7μH to 15μH
	A1A1R2 from 30.1ku to 68.1ku
	A1A1R3 from 1ku to 560u.
	Added A1A1CR3, BB109
	Added A1A1CR4, BB109
	Added A1A1CR5 BB109
	Added A1A1C24, 8pF
	Added A1A1R16, 47u
	Added A1A1R17, 330u
	Added A1A1R18, 820u
		635-0890-002, REV F and above.

A7	Added A1R19, 270u
	Added A1R20, 270u
	Added A1R21, 18u
		635-1760-001, REV D and above.

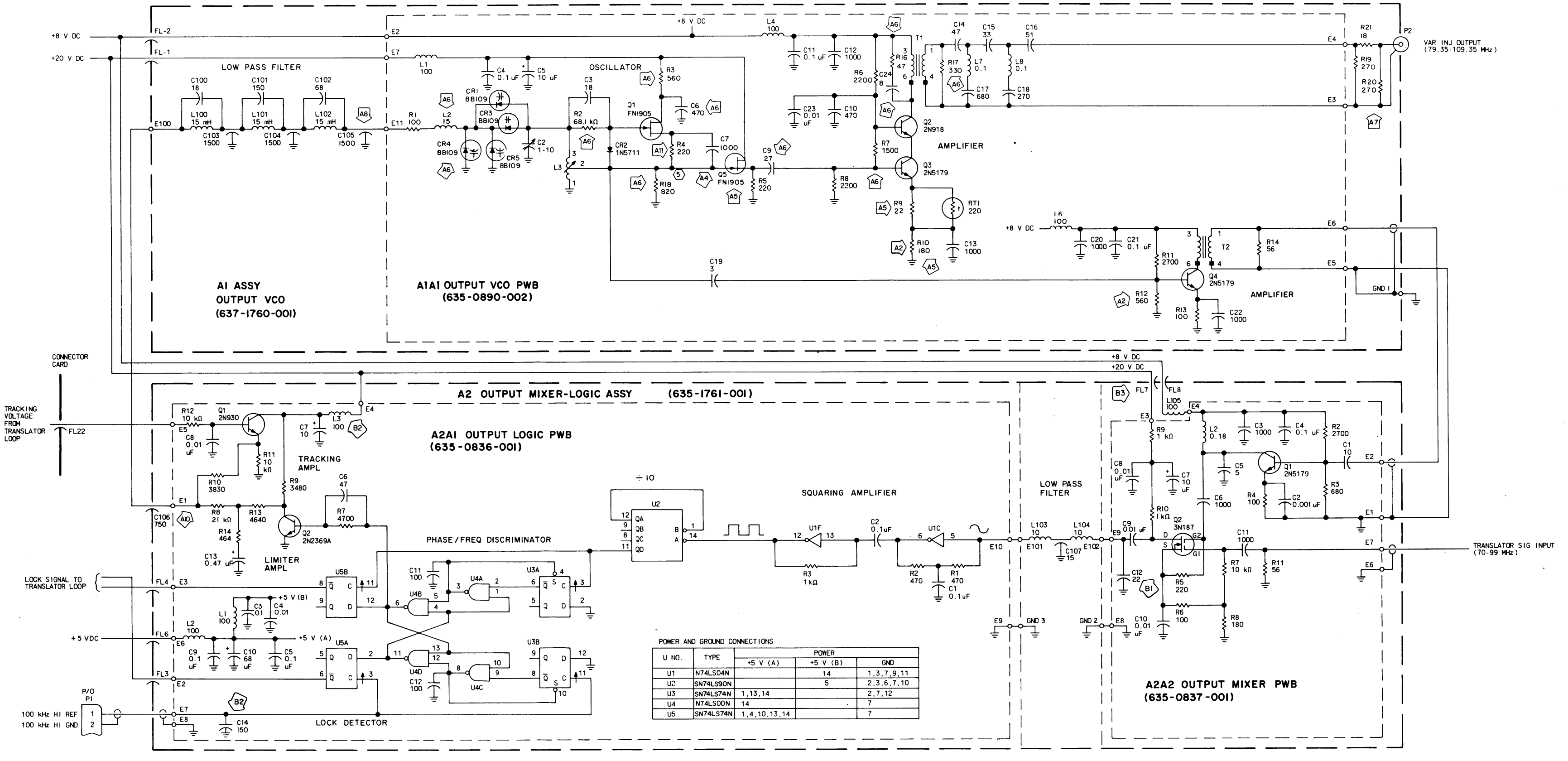
A8	Changed A1C105 from 750pF to 1500pF.	637-1760-001, REV E and above.
A9	Changed A3L110 from 10mH to 9.3mH	637-1763-001, REV D and above.
A10	Changed A2A1R8 from 33.2ku to 21ku.	635-0836-001, REV B and above.
A11	Changed A1A1R4 from 1ku variable to; test select of 150u to 560u.	635-0890-002 REV G and above.
B1	Added A2A2C12, 22pF.	635-0837-001 REV B and above.
B2	Added A2A1C14, 150pF. Changed A2A1L3 from 4.7uH to 100μH.	635-0836-001 REV C and above.
B3	Added A2L105, 100μH.	637-1761-001 REV E and above.



MODIFICATION HISTORY (Cont)

REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
B4	Added A3C116, 33pF.	637-1763-001 REV F and above.

Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 3A)



Synthesizer Output, Schematic Diagram
Figure 9 (Sheet 4)